Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DANIEL WATKINS

Appeal No. 2004-2113
Application No. 09/363,311

ON BRIEF

Before HAIRSTON, LEVY, and BLANKENSHIP, Administrative Patent Judges.

LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-20, which are all of the claims pending in this application.

BACKGROUND

Appellant's invention relates to a functional-pattern management system for device verification. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced as follows:

1. A system for device verification, wherein the system comprises

a profile generation module configured to provide a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vector (hereafter a "test pattern"), wherein the pattern profile includes a human-intelligible description of aspects of the test pattern, wherein the aspects are specified by a profile mode;

a coverage measurement module configured to process the pattern profile to produce analysis results indicative of coverage provided by the test pattern, wherein the profile generation module is further configured to process the analysis results to provide an improved pattern profile; and

a pattern generation module configured to receive the improved pattern profile and to convert the improved pattern profile into a test pattern for verifying device performance.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Valind	5,684,808	Nov. 4, 1997
Kurosaka et al. (Kurosaka)	5,949,691	Sep. 7, 1999 (filed Aug. 14, 1997)
McNamara et al. (McNamara)	6,141,630	Oct. 31, 2000 (filed Aug. 7, 1997)

Claims 1-6, 8, 9, 11-14 and 16-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurosaka in view of McNamara.

Claims 7, 10 and 15 stand rejected under 35 U.S.C. § 103(a)

as being unpatentable over Kurosaka in view of McNamara and further in view of Valind.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellant regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 12, mailed December 2, 2003) for the examiner's complete reasoning in support of the rejections, and to appellant's brief (Paper No. 11, filed August 20, 2003) for appellant's arguments thereagainst. Only those arguments actually made by appellant have been considered in this decision. Arguments which appellant could have made but chose not to make in the brief have not been considered. See 37 CFR 41.37(c).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejections advanced by the examiner, and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellant's arguments set forth in the brief along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

Upon consideration of the record before us, we reverse, essentially for the reasons set forth by appellant. We observe appellant's statement (brief, page 6) that claims 1-20 stand together. However, because appellant is entitled procedurally to consideration of at least one claim for each ground of rejection, we select claim 1 as representative of the claims rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurosaka in view of McNamara, and select claim 7 as representative of the claims rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurosaka in view of McNamara and further in view of Valind. We begin with claim 1.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal,

Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

The examiner's position (answer, page 3) is that the data input 101 is a profile generation module that is configured to provide a profile pattern (intermediate format data file 106) which represents a test pattern. The examiner further asserts (answer, page 4) that profile generation module 101 of Kurosaka is configured to provide an improved pattern profile. Additionally, the examiner takes the position (id.) that point detection section 102 of Kurosaka reads on the pattern generation

module, and is configured to receive the improved pattern profile and convert the improved pattern profile into a test pattern. The examiner asserts (id.) that Kurosaka does not teach that the test pattern is a time sequence of input signal vectors with an associated sequence of output signal vectors. To overcome this deficiency of Kurosaka, the examiner turns to McNamara for a teaching of a test pattern as a time sequence of input signal vectors and an associated sequence of output signal vectors.

Appellant notes (brief, page 7) that "[i]ndependent claim 1 recites in part: `a pattern profile that represents a sequence of input signal vectors with an associated sequence of output signal vectors (hereafter a `test pattern'),'" and asserts that intermediate format data file 106 does not meet the claimed pattern profile that represents a test pattern. It is argued (id.) that data file 106, in the intermediate format, is provided to store detailed circuit information, and that Kurosaka uses this file to store circuit information for two circuits that he wishes to compare using a point-detection algorithm. Appellant maintains that no sequence of input signal vectors is represented by data file 106. With regard to McNamara, appellant asserts (id.) that McNamara teaches the use of a test generator that constructs a set of test vectors from a circuit design coded in a circuit design language. The test generator interprets the

circuit design as a series of blocks connected by a series of transition arcs to form a state diagram. A first set of vectors is used to cause each block to be visited and each transition arc to be taken. A second set of vectors is also constructed to ensure that user-selected paths are taken. It is argued (id.) that as in Kurosaka, the data structures represent the circuit design, and not a test pattern. Appellant finds (id.) from their review of McNamara, no teaching or suggestion of a test pattern profile.

From our review of Kurosaka, we find that data input section 101 inputs circuit data of the circuits to be verified, and converts the data into an intermediate format that is independent of the technology (col. 6, lines 31-35). A corresponding point detection section 102 detects the points in the circuits to be detected (col. 6, lines 35-37). A circuit partitioning section 103, referring to the detection results from the corresponding point detection 102, partitions the circuits to be verified, so as to prepare sub-circuits (col. 6, lines 37-40). An equivalence checking section 104 collates the sub-circuits prepared by circuit partitioning section 103 (col. 6, lines 40-42). Data input section 101 reads data from circuit data 105 and library 110, and converts them into a data file 106 in the intermediate format, and outputs them to corresponding point detection circuit 102 and circuit partitioning section 103. Circuit data 105

describes the circuits to be verified. Data file 106 stores detailed circuit information (col. 6, line 60 through col. 7, line 9). The corresponding point detection section 102 stores the corresponding point detection algorithms. It reads data file 106, and using one of the corresponding point detection algorithms, detects the points in the two circuits to be verified, and prepares corresponding point information 108 (col. 7, lines 10-16).

In addition, although it has not been brought to our attention by either the examiner or the appellant, we find from our review of Kurosaka that the reference discloses the use of test patterns generated by an Automatic Test Pattern Generator. Kurosaka discloses (col. 8, lines 41-49) that:

> The equivalence checking section 104 compares the data of the corresponding subcircuits among the subcircuit data 109 prepared by the circuit partitioning section 103 and writes the comparison result to the corresponding point information 108. At the equivalence checking section 104, circuits are compared by a verification method using BDD (Binary Decision Diagram) or a verification method with simulation generating test patterns using ATPG (Automatic Test Pattern Generator) for example.

However, because the generated test pattern is used in checking the equivalence of the data of the corresponding sub-circuits prepared by the circuit partitioning section 103, we do not agree with the examiner (answer, page 4) that data file 106

constitutes a pattern profile that represents a test pattern; i.e., since a test pattern is used by the equivalence checking section in Kurosaka, the intermediate format data file 106 is not a pattern profile that represents a test pattern. We agree with appellant that Kurosaka describes a circuit instead. In addition, because corresponding point detection section 102 is used to detect points on the circuit that need to be verified (col. 7, line 13, underlining added), we find that the corresponding point detection section 102 is not a pattern generation module that is configured to receive an improved pattern profile and convert the improved pattern profile into a test pattern, as recited in claim 1. Thus, we find that the Kurosaka reference does not correlate with the limitations of claim 1 as advanced by the examiner. Because the examiner has misapplied the Kurosaka reference to the claim limitations, we find that even if McNamara does disclose a test pattern that represents a sequence of input signal vectors with an associated sequence of associated output signal vectors, as advanced by the examiner (answer, page 4), we find no manner in which an artisan could combine the teachings of Kurosaka and McNamara to arrive at the invention set forth in claim 1. Accordingly, from all of the above, we find that the examiner has failed to establish a prima facie case of obviousness of claim 1. The rejection of claim 1,

and claims 2-6, 8 and 9, dependent therefrom, is therefore reversed.

We turn next to independent claims 11 and 17. As independent claims 11 and 17 both recite pattern profiles that represent test patterns, we find that the examiner has failed to establish a prima facie case of obviousness of claims 11 and 17. Accordingly, the rejection of claims 11 and 17, and claims 12-14, 16, and 18-20, dependent therefrom, is reversed.

We turn next to the rejection of dependent claims 7, 10, and 15 under 35 U.S.C. § 103(a) as being unpatentable over Kurosaka in view of McNamara and further in view of Valind. We reverse the rejection of claims 10, 15 and 17 because Valind does not make up for the deficiencies of the basic combination of Kurosaka and McNamara. Accordingly, the rejection of claims 10, 15 and 17 is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-20 under 35 U.S.C. § 103(a) is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136 (a).

REVERSED

KENNETH W. HAIRSTON
Administrative Patent Judge

STUART S. LEVY
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

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